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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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YING TUO CROSBY HEAFEY ROACH & MAY P O BOX 7936 SAN FRANCISCO, CA 941207936			PHAN, THAI Q	
			ART UNIT	PAPER NUMBER
			2128	

DATE MAILED: 11/03/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 09/340,580	Applicant(s) IP, CHUNG-WAH NORRIS	
	Examiner Thai Q. Phan	Art Unit 2128	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 19 July 2004.
- 2a) ☒ This action is **FINAL**. 2b) ☐ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-45 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1-41 is/are rejected.
- 7) ☒ Claim(s) 42-45 is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on _____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. _____.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- * See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|--|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____ |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152) |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date _____ | 6) <input type="checkbox"/> Other: _____ |

DETAILED ACTION

This Office action is in response to applicants' amendment filed on 07/19/2004. Claims 42-45 are newly added. Claims 1-45 are pending in the Action.

Drawings

The drawings are acceptable for examination.

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

2. Claims 1-41 are rejected under 35 U.S.C. 103(a) as being unpatentable over Gilbertson, US patent no. 6,510,405 B in view of Trimberger (US patent no. 5,650,946).

As per claim 1, Gilbertson discloses a method and system for simulating and verifying circuit design with feature limitations substantially similar to the claimed invention (Summary of the Invention). According to Gilbertson, the simulation method includes steps of dividing all possible design states for the design into a plurality of interest validation regions (col. 4, line 66 to col. 5, line 14), recording simulation data in virtual history stack to produce corrective action and valid stimulus test vector (Fig. 5, col. 6, lines 14-44, col. 8, lines 33-60, for example) from the first analysis step, and generating a new set of stimuli by

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examining from error violation data, for example and performing the simulation process using the new set of stimuli data as claimed (cols. 8-9). Gilbertson discloses virtual history stack for storing historical simulation data or record for simulation. Gilbertson does not expressly disclose the claimed feature of simulation history. Such feature is however known in the art. In fact, Trimberger teaches a logic simulation. The simulator generates simulation stimuli based on simulation data or simulation history data for efficient logic simulation (col. 4, lines 38-62, col. 6, line 32 to col. 7, line 42, for example) such as increasing design verification speed and reducing design simulation time (col. 4, lines 1-35, col. 8, lines 20-25).

This would motivate practitioner in the art at the time of the invention was made to modify Gilbertson virtual history stack for historical simulation data by combining the teaching of Trimberger of generating stimuli data applied to logic circuit based on simulation history in order to efficiently simulate the design circuit as taught in Trimberger.

As per claim 2, Trimberger teaches deriving a new set of stimulus data or forcing functions from previously recorded simulation data or history of simulation data.

As per claim 3, Gilbertson discloses a sequence of stimulus vector or portion of test sequence would be used to apply to region verification efficiency (col. 3, lines 1-17, col. 4, lines 2-8, col. 5, for example).

As per claim 4, Gilbertson discloses a method and system for simulating and verifying circuit design with feature limitations substantially similar to the

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claimed invention (Summary of the Invention). According to Gilbertson, the simulation method includes steps of dividing all possible design states for the design into a plurality of interest validation regions (col. 4, line 66 to col. 5, line 14), recording simulation data in virtual history stack to produce corrective action and valid stimulus test vector (Fig. 5, col. 6, lines 14-44, col. 8, lines 33-60, for example) from the first analysis step, and generating a new set of stimuli by examining from error violation data, for example and performing the simulation process using the new set of stimuli data as claimed (cols. 8-9). Gilbertson discloses virtual history stack for storing historical simulation data or record for simulation. Gilbertson does not expressly disclose the claimed simulation history for generation of input simulation. Such feature is however known in the art. In fact, Trimberger teaches a simulation history used to generate new or transform stimuli for logic simulation. The simulator generates or transforms simulation stimuli based on simulation data or simulation history data for efficient logic simulation (col. 4, lines 38-62, col. 6, line 32 to col. 7, line 42, for example) such as increasing design speed, reducing design simulation time, etc. (col. 4, lines 1-35).

This would motivate practitioner in the art at the time of the invention was made to modify Gilbertson virtual history stack for historical simulation data by combining the teaching of Trimberger of generating stimuli data applied to logic circuit based on simulation history in order to efficiently simulate the design circuit as taught in Trimberger.

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As per claim 5, Gilbertson discloses a simulation efficiency and state coverage during simulation (col. 6, lines 54-67, col. 7, lines 22-53, col. 8, lines 34-60, for example).

As per claim 6, Gilbertson discloses step: generating new stimuli, test vectors, data transformation for use in valid test (col. 3, lines 7-34, cols. 7-9).

As per claim 7, Gilbertson discloses occurrence of the taken stimulus in the current validation (Fig. 4, col. 7, line 62 to col. 8, line 12), using the current stimulus for subsequent steps if needed to valid a test (see above and col. 8, lines 13-43), and timing restriction rules such as occurrence rules, check states, etc. for stimulus data applied for test validation (cols. 7-9).

As per claim 8, Gilbertson discloses stimulus specification, and state legal for valid test (col. 4, lines 5-8, col. 6, lines 15-35, cols. 7-9).

As per claim 9, Gilbertson discloses current update for simulation test data display.

As per claim 10, due to the similarity of claim 10 to claim 1, and Gilbertson discloses a method and system for simulating and verifying circuit design with feature limitations substantially similar to the claimed invention (Summary of the Invention). According to Gilbertson, the simulation method includes steps of dividing all possible design states for the design into a plurality of interest validation regions (col. 4, line 66 to col. 5, line 14), recording simulation data in virtual history stack to produce corrective action and valid stimulus test vector (Fig. 5, col. 6, lines 14-44, col. 8, lines 33-60, for example) from the first analysis step, and generating a new set of stimuli by examining from error violation data,

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for example and performing the simulation process using the new set of stimuli data as claimed (cols. 8-9). Gilbertson discloses virtual history stack for storing simulation data for the design verification. Gilbertson does not expressly disclose the claimed feature of simulation history. Such feature is however known in the art. In fact, Trimberger teaches a logic simulation. The simulator generates simulation stimuli based on simulation data or simulation history data for efficient logic simulation (col. 4, lines 38-62, col. 6, line 32 to col. 7, line 42, for example) such as increasing design speed, reducing design simulation time, etc. (col. 4, lines 1-35).

This would motivate practitioner in the art at the time of the invention was made to modify Gilbertson virtual history stack for historical simulation data by combining the teaching of Trimberger of generating stimuli data applied to logic circuit based on simulation history in order to efficiently simulate the design circuit as taught in Trimberger.

As per claims 11 and 12, Gilbertson discloses an occurrence of the taken stimulus in the current validation (cols. 4, 7 and 8), using the current stimulus for subsequent steps if needed to valid a test (col. 8, lines 13-43), and timing restriction rules such as occurrence rules, check states, etc. for stimulus data applied for test validation (cols. 7-9).

As per claim 13, Gilbertson discloses a method and system for simulating and verifying circuit design with feature limitations substantially similar to the claimed invention (Summary of the Invention). According to Gilbertson, the simulation method includes steps of dividing all possible design states for the

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design into a plurality of interest validation regions (col. 4, line 66 to col. 5, line 14), recording simulation data in virtual history stack to produce corrective action and valid stimulus test vector (Fig. 5, col. 6, lines 14-44, col. 8, lines 33-60, for example) from the first analysis step, and generating a new set of stimuli by examining from error violation data, for example and performing the simulation process using the new set of stimuli data as claimed (cols. 8-9). Gilbertson discloses the virtual history stack and emulation of the virtual stack data for generating an efficient simulation. Gilbertson does not expressly disclose generating a new set of stimuli by examining the existing stimuli based on the simulation history as claimed. Such feature is however known in the art. In fact, Trimberger teaches a logic simulation. The simulator generates simulation stimuli based on simulation data or simulation history data for efficient logic simulation (col. 4, lines 38-62, col. 6, line 32 to col. 7, line 42, for example) such as increasing design verification speed and reducing design simulation time (col. 4, lines 1-35, col. 8, lines 2-25).

This would motivate practitioner in the art at the time of the invention was made to modify Gilbertson virtual history stack for historical simulation data by combining the teaching of Trimberger of generating stimuli data applied to logic circuit based on simulation history in order to efficiently simulate the design circuit as taught in Trimberger.

As per claims 14-18, due to the similarities of claims 14-18 to claims 1, 3 and 7 above, claims 14-18 are also rejected under the same rationales as set forth.

As per claim 19, Gilbertson discloses method and system for simulating and verifying circuit design with feature limitations substantially similar to the claimed invention (Summary of the Invention). According to Gilbertson, the simulation method includes steps of dividing all possible design states for the design into a plurality of interest validation regions (col. 4, line 66 to col. 5, line 14), recording simulation data in virtual history stack to produce corrective action and valid stimulus test vector (Fig. 5, col. 6, lines 14-44, col. 8, lines 33-60, for example) from the first analysis step, and generating a new set of stimuli by examining from error violation data, for example and performing the simulation process using the new set of stimuli data as claimed (cols. 8-9). Gilbertson discloses virtual history stack for storing historical simulation data or record for simulation. Gilbertson does not expressly disclose the claimed feature of simulation history. Such feature is however known in the art. In fact, Trimberger teaches a logic simulation. The simulator generates simulation stimuli based on simulation data or simulation history data for efficient logic simulation (col. 4, lines 38-62, col. 6, line 32 to col. 7, line 42, for example) such as increasing design speed, reducing design simulation time, etc. (col. 4, lines 1-35).

This would motivate practitioner in the art at the time of the invention was made to modify Gilbertson virtual history stack for historical simulation data by combining the teaching of Trimberger of generating stimuli data applied to logic circuit based on simulation history in order to efficiently simulate the design circuit as taught in Trimberger.

As per claim 20, Gilbertson discloses means for deriving a new set of stimulus data from previously recorded simulation data and emulation of virtual stacks, or claimed simulation history data in order to verify the circuit design (col. 6, lines 14-34, lines 54-64, col. 7, lines 36-45, for example).

As per claim 21, Gilbertson discloses means for changing the order in the existing stimuli based the previously recorded simulation data or simulation history as claimed (col. 3, and col. 5),

As per claim 22, Gilbertson discloses method and system for simulating and verifying circuit design with feature limitations substantially similar to the claimed invention (Summary of the Invention). According to Gilbertson, the simulation method includes steps of dividing all possible design states for the design into a plurality of interest validation regions (col. 4, line 66 to col. 5, line 14), recording simulation data in virtual history stack to produce corrective action and valid stimulus test vector (Fig. 5, col. 6, lines 14-44, col. 8, lines 33-60, for example) from the first analysis step, and generating a new set of stimuli by examining from error violation data, for example and performing the simulation process using the new set of stimuli data as claimed (cols. 8-9). Gilbertson discloses virtual history stack for storing historical simulation data or record for simulation. Gilbertson does not expressly disclose generating a new set of stimuli by examining the existing stimuli based on the simulation history as claimed. Such feature is however known in the art. In fact, Trimberger teaches a logic simulation. The simulator generates simulation stimuli based on simulation data or simulation history data for efficient logic simulation (col. 4, lines 38-62,

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col. 6, line 32 to col. 7, line 42, for example) such as increasing design speed, reducing design simulation time, etc. (col. 4, lines 1-35).

This would motivate practitioner in the art at the time of the invention was made to modify Gilbertson virtual history stack for historical simulation data by combining the teaching of Trimberger of generating stimuli data applied to logic circuit based on simulation history in order to efficiently simulate the design circuit as taught in Trimberger.

As per claims 23-27, claims 23-27 are directed to system for performing steps and system for performing method claims 5-9, claims 23-27 are thus rejected under the same rationales as set forth.

As per claim 28, Gilbertson discloses method and system for simulating and verifying circuit design with feature limitations substantially similar to the claimed invention (Summary of the Invention). According to Gilbertson, the simulation method includes steps of dividing all possible design states for the design into a plurality of interest validation regions (col. 4, line 66 to col. 5, line 14), recording simulation data in virtual history stack to produce corrective action and valid stimulus test vector (Fig. 5, col. 6, lines 14-44, col. 8, lines 33-60, for example) from the first analysis step, and generating a new set of stimuli by examining from error violation data, for example and performing the simulation process using the new set of stimuli data as claimed (cols. 8-9). Gilbertson discloses virtual history stack for storing historical simulation data or record for simulation. Gilbertson does not expressly disclose generating a new set of stimuli by examining the existing stimuli based on the simulation history as

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claimed. Such feature is however known in the art. In fact, Trimberger teaches a logic simulation. The simulator generates simulation stimuli based on simulation data or simulation history data for efficient logic simulation (col. 4, lines 38-62, col. 6, line 32 to col. 7, line 42, for example) such as increasing design speed, reducing design simulation time, etc. (col. 4, lines 1-35).

This would motivate practitioner in the art at the time of the invention was made to modify Gilbertson virtual history stack for historical simulation data by combining the teaching of Trimberger of generating stimuli data applied to logic circuit based on simulation history in order to efficiently simulate the design circuit as taught in Trimberger.

Similarly, claims 29-30 are directed to system for performing steps of method claims 2-3 and 7 above, claims 29-30 are thus rejected in like manner.

As per claims 31-36, claims 31-36 are directed to system for performing steps of claims 13-16 above. Gilbertson discloses a method and system for simulating and verifying circuit design with feature limitations substantially similar to the claimed invention (Summary of the Invention). According to Gilbertson, the simulation method includes steps of dividing all possible design states for the design into a plurality of interest validation regions (col. 4, line 66 to col. 5, line 14), recording simulation data in virtual history stack to produce corrective action and valid stimulus test vector (Fig. 5, col. 6, lines 14-44, col. 8, lines 33-60, for example) from the first analysis step, and generating a new set of stimuli by examining from error violation data, for example and performing the simulation process using the new set of stimuli data as claimed (cols. 8-9). Gilbertson

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discloses the virtual history stack for storing simulation data. Gilbertson does not expressly disclose generating a new set of stimuli by examining the existing stimuli based on the simulation history as claimed. Such feature is however known in the art. In fact, Trimberger teaches a logic simulation. The simulator generates simulation stimuli based on simulation data or simulation history data for efficient logic simulation (col. 4, lines 38-62, col. 6, line 32 to col. 7, line 42, for example) such as increasing design speed, reducing design simulation time, etc. (col. 4, lines 1-35).

This would motivate practitioner in the art at the time of the invention was made to modify Gilbertson virtual history stack for historical simulation data by combining the teaching of Trimberger of generating stimuli data applied to logic circuit based on simulation history in order to efficiently simulate the design circuit as taught in Trimberger.

As per claim 37, Gilbertson discloses stimuli vector specified for circuit simulation (Figs. 4 and 5, col. 6, lines 15-35, lines 45-50, cols. 7-8).

As per claim 38, Gilbertson discloses parts of system design imply the claimed step of dividing design states into a plurality of regions (Fig. 1, block 12, and col. 5, lines 1-8, for example). Gilbertson also discloses storing simulation results in various memory regions or in memory stacks as claimed.

As per claim 39, Gilbertson discloses mapping function for mapping simulation values and the results of simulation are stored in virtual history stack for tracing (Figs. 4, 5, col. 6, lines 14-44, cols. 7-8, for example).

As per claims 40-41, Gilbertson discloses logic design simulation and validation with virtual history stack for functional mapping state values relevant to particular simulation events as claimed.

Allowable Subject Matter

1. Claims 42-45 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.
2. The claims further require a plurality of hashing means, comprising one hashing means corresponding to each validation region; wherein each hashing means comprises hashing representative state values of the corresponding validation region, a hash table for the corresponding validation region, means for storing the hashed values in the corresponding hash table, and retrieving means for retrieving simulation history stored in the hashed representative state values using the corresponding hash table and a corresponding hash key. The prior art does not expressly disclose such feature limitations as in the claimed invention.

Response to Arguments

1. Applicant's arguments filed 07/19/2004 have been fully considered but they are not persuasive.
2. In response to applicants' argument Gilbertson does not expressly disclose or suggest a step of generating stimuli for test generation, the examiner disagrees with. Gilbertson discloses a step of generating test values of the selected signals (col. 4, lines 18-28). In other words, the test signal values or stimuli values as claimed is generated based on the virtual history stacks for

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particular events or system part. The examiner reminds applicants update data is not similar to generate stimuli data as applicants argued in page 15.

3. In response to applicants' Gilbertson does not disclose or suggest generation of new stimuli data (page 15, second paragraph), the examiner disagrees with. Gilbertson discloses input data is generated for device testing by examining from error violation data, for example, and performing the simulation process using the new set of stimuli data as claimed (cols. 8-9).

4. In response to applicants' argument the combined prior art fails to disclose or suggest generating a (new) set of stimuli by examining the existing stimuli based on the simulation history (page 16, paragraph 1), the examiner disagrees with. In fact, Trimberger teaches a simulation history for logic simulation. The simulator generates (new) simulation stimuli based on simulation data or simulation history data for efficient logic simulation (col. 4, lines 38-62, col. 6, line 32 to col. 7, line 42, for example) such as increasing design verification speed and reducing design simulation time (col. 4, lines 1-35, col. 8, lines 20-25).

This would motivate practitioner in the art at the time of the invention was made to modify Gilbertson virtual history stack for historical simulation data by combining the teaching of Trimberger of generating stimuli data applied to logic circuit based on simulation history in order to efficiently simulate the design circuit as taught in Trimberger.

Conclusion

1. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

2. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Thai Q. Phan whose telephone number is 703-305-3812.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Jean Homere can be reached on 703-308-6647. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

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3. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Oct. 25, 2004

A handwritten signature in black ink, appearing to read 'Thai Phan', is positioned above the printed name.

Thai Phan

Patent Examiner

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